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AUTOMATIC-BIAS AMPLIFIER CIRCUIT

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CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority to U.S. Provisional Patent Application Serial No. 60/419,027, filed on October 15, 2002, which is incorporated herein by reference in its entirety. This application also claims priority to U.S. Patent Application Nos. 10/459,239, entitled "Accurate Power Detection for a Multi-Stage Amplifier," filed on June 10, 2003 (Attorney Docket TRQ-12924), and 10/607,959, entitled "Continuous Bias Circuit and Method for an Amplifier," filed on June 27, 2003 (Attorney Docket No. TRQ-12905), both of which are incorporated herein by reference in their respective entireties.

BACKGROUND OF THE INVENTION

1. Technical Field

[0002] The present disclosure relates to amplifiers, such as amplifiers that amplify radio frequency (RF) signals.

2. Discussion of the Related Art

[0003] Amplifiers are often used in portable, battery operated devices, such as cellular telephone and personal digital assistant (PDA) devices, to amplify RF signals. Performance of such an amplifier is largely judged by the amplifier's linearity and power efficiency. Linearity requires proportional amplification with low distortion over a wide

dynamic range. Power efficiency requires low power consumption over the dynamic range. Typically, linearity is achieved at a cost to power efficiency, or vice versa.

[0004] For instance, in order to provide linearity over a wide dynamic range, it is conventional to bias the amplifier to operate most efficiently at a single output power level in the dynamic range. Typically, the selected single output power level is the level at which, statistically, the amplifier most commonly operates. This is effective for providing linearity over the dynamic range, but only provides power efficiency at the single output power level.

[0005] An alternative approach to improve power efficiency, while maintaining linearity, is to provide multiple amplifier stages and to combine their outputs. Such an approach allows a designer to separately optimize the power efficiency of each of the multiple amplifier stages. While this approach constitutes an improvement over biasing for a single output power level, efficiency is still improved at only a small number of the possible output power levels.

[0006] Therefore, a need exists to improve the power efficiency of an amplifier while still maintaining linearity over a wide dynamic range of operation.

SUMMARY OF THE DISCLOSURE

[0007] The present invention includes a method and a circuit for operating and controlling an amplifier, so that the current consumption of the amplifier is automatically optimized over all output power levels, while maintaining a desired, high degree of linearity.

[0008] In one embodiment, an automatic-bias amplifier circuit includes an amplifier and a feedback loop coupled to the amplifier. A signal passes through the amplifier on a signal path, is amplified therein, and is output by the amplifier at a selected power level. The feedback loop includes a power detector coupled to the signal path for sampling the signal and a bias circuit coupled between the power detector and a bias input of the amplifier. The power detector may be coupled to the signal path for sampling at one or more points, e.g., at the amplifier output, or at one or more internal nodes of the amplifier. The power detector samples the signal on the signal path and outputs, to downstream elements of the feedback loop, an analog, i.e., continuously-varying, voltage signal reflective of the detected power of the signal. The bias circuit causes the amplifier to draw an analog quiescent current from a fixed-voltage level DC voltage source. The quiescent current varies proportionally with the analog voltage signal output by the power detector. Accordingly, the current consumption of the amplifier is self-optimized for the power of the signal being output by the amplifier.

[0009] The automatic-bias amplifier circuit may be part of a wireless communications device, such as a cellular phone or a personal digital assistant device. A baseband processor of the wireless communications device generates a data signal, which is converted to a RF signal and provided to a preamplifier on the signal path. The RF signal is amplified by the preamplifier, and is then provided to the automatic-bias amplifier. The baseband processor also continuously determines a desired power level of the signal to be output by the automatic-bias amplifier. The baseband processor continuously adjusts the gain of the preamplifier so that, at any given time, the RF signal provided to the automatic-bias amplifier circuit by the preamplifier will have a power level sufficient to allow the automatic-bias amplifier circuit to further amplify the RF signal to the

desired power level. Meanwhile, the power detector of the automatic-bias amplifier circuit samples the RF signal on the signal path of the amplifier, and provides an analog voltage signal reflective of the power of the sampled RF signal to the feedback loop. The bias circuit of the feedback loop causes the automatic-bias amplifier to draw an analog quiescent current from a fixed-level DC voltage supply. The quiescent current varies proportionally with the analog voltage signal. The current consumption of the amplifier is thereby optimized for all output power levels specified by the baseband processor, while maintaining a desired degree of linearity.

[0010] These and other aspects of the present invention will become more apparent through consideration of the accompanying drawings and the following detailed description of the exemplary embodiments

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] Figure 1 is a block diagram of an embodiment of a radio frequency transmission circuit that includes an automatic-bias amplifier circuit, in accordance with the present invention.

[0012] Figure 2 is a block diagram of an embodiment of the automatic-bias amplifier circuit of Fig. 1.

[0013] Figure 3 is a diagram of a conventional power detector that may be used in accordance with the present invention.

[0014] Figure 4 is diagram of an alternative power detector that may be used in accordance with the present invention.

[0015] Figure 5 is a schematic diagram of an embodiment of a linearizer circuit.

[0016] Figure 6 is a schematic diagram of an embodiment of an amplifier bias circuit, in accordance with the present invention.

[0017] Figure 7 is a graph of linearity versus output power of a simulated automatic-bias amplifier.

[0018] Figure 8 is a graph of current consumption versus output power for a simulated automatic-bias amplifier.

[0019] In the present disclosure, like objects that appear in more than one figure are typically provided with like reference numerals.

DETAILED DESCRIPTION

[0020] The present invention includes an automatic-bias amplifier circuit that includes an amplifier, and a feedback loop that automatically regulates the amplifier's current consumption.

[0021] The particular example discussed below relates to an automatic-bias amplifier circuit used to amplify RF signals in a wireless communications device, but practitioners will appreciate that the teachings herein may be used with respect to other amplifier applications.

[0022] Figure 1 is a simplified block diagram of an embodiment of a radio frequency transmission circuit 1 in accordance with the present invention. Included within radio frequency transmission circuit 1 is an automatic-bias amplifier circuit 5, which includes amplifier 35 and a feedback loop 37 that is disposed between a sampling point on a signal path 21, e.g., at the output 35b of amplifier 35, and a bias input of amplifier 35, as is discussed below. Feedback loop 37 includes a power detector 65 and a bias circuit 40. Bias circuit 40 is coupled to power detector 65 and ultimately receives the output of power detector 65.

[0023] As an example, radio frequency transmission circuit 1 may be in a battery-operated wireless communications device, e.g., a cellular telephone or PDA device, that transmits and receives RF signals. Radio frequency transmission circuit 1 may operate according to any number of communication standards, including, but not limited to, the CDMA, WCDMA, GSM, or AMPS standards.

[0024] Radio frequency transmission circuit 1 includes a baseband processor 10 that receives data, e.g., voice and/or packet data, at input 15. Based on this data input, baseband processor 10 outputs an encoded data signal 18 to a modulator 20. Modulator 20 modulates the data signal 18 to produce a RF signal 30. The RF signal 30 is provided to a preamplifier 25, which amplifies the RF signal 30 and provides the RF signal 30 to input 35a of amplifier 35. Amplifier 35 further amplifies the RF signal 30, and outputs the further-amplified RF signal 30 to antenna 60 via output 35b of amplifier 35.

Amplifier 35 may be a single stage amplifier, or a multi-stage (i.e., two or more stages) amplifier. Antenna 60 broadcasts RF signal 30. Signal path 21, on which RF signal 30 passes, extends from the baseband processor 10 port that outputs data signal 18 though modulator 20, preamplifier 25 and amplifier 35 to antenna 60.

[0025] Baseband processor 10 also outputs an analog, i.e., continuously varying, voltage signal 50 that is provided to preamplifier 25 via line 11. Voltage signal 50 has a magnitude determined in real time by baseband processor 10 to achieve a desired power level in the RF signal 30 that is output by amplifier 35 and broadcast via antenna 60.

[0026] In a wireless communications embodiment, baseband processor 10 determines the magnitude of voltage signal 50 in real time by decoding an output power instruction that baseband processor 10 receives at its input 15 from an external source, such as a base station in RF communication with a mobile unit (e.g., a cellular phone) that includes radio frequency transmission circuit 1. The output power instruction is available in most systems that operate according to the WCDMA, CDMA, Global System for Mobile Communications (GSM), and the Advanced Mobile Phone Service (AMPS) standards.

[0027] At preamplifier 25, voltage signal 50 is used to adjust the gain of preamplifier 25 using any of several methods. For instance, voltage signal 50 may be input to a bias circuit that causes the pre-amplifier bias voltage to vary. The magnitude of voltage signal 50 is selected by baseband processor 10 so that preamplifier 25 will provide amplifier 35 with an input RF signal 30 having just the right amount of power for amplifier 35 to further amplify the RF signal 30 to the desired output power level, as was previously-determined by baseband processor 10, for broadcast via antenna 60.

[0028] Baseband processor 10 accounts for the characteristics of amplifier 35 in determining the value of analog voltage signal 50. In one embodiment, baseband processor 10 relies on a software model of amplifier 35, and determines the value of analog voltage signal 50 based on the model. For instance, the model includes the expected amount of amplification by amplifier 35.

[0029] In an alternative embodiment, shown by dash lines in Fig. 1, baseband processor 10 is coupled to power detector 65 by feedback line 12, and receives an analog voltage signal 70 from power detector 65 via feedback line 12. As discussed below, voltage signal 70 is reflective of the power the RF signal 30 at the point of sampling, e.g., at output 35b of amplifier 35. In this alternative embodiment, baseband processor 10 uses voltage signal 70 to determine the value of analog voltage signal 50 in real time. In other words, baseband processor 10 uses the sampled RF signal 30 to determine the value of analog voltage signal 50.

[0030] As mentioned, feedback loop 37 includes a power detector 65 that is coupled to signal path 21. In the embodiment of Fig. 1, input 65a of power detector 65 is coupled to signal path 21 at output 35b of amplifier 35, prior to antenna 60. However, as discussed below, power detector 65 alternatively may be coupled to signal path 21 at one or more internal nodes of amplifier 35, or both at the output 35b and at one or more internal nodes of amplifier 35. Power detector 65 can be coupled to the signal path 21 by a directional coupler or inductive coupling, or the like.

[0031] Power detector 65 samples the power of RF signal 30 on signal path 21, and provides at its output 65b an analog voltage signal 70 that reflects the detected power of RF signal 30. The analog voltage signal 70 is provided to downstream elements of feedback loop 37. In the embodiment of Fig. 1, bias circuit 40 receives the analog voltage signal 70 from output 65b of power detector 65, and uses voltage signal 70 to control the current consumption of amplifier 35. (Note that, while we say that bias circuit 40 receives and uses the analog voltage signal 70, this includes receiving and using either the actual analog voltage signal 70 output by power detector 65, or a signal derived therefrom, which may be, e.g., a shifted and/or linearized signal.)

[0032] In particular, bias circuit 40 controls an amount of an analog quiescent current 45 that amplifier 35 draws from a fixed-level DC voltage source Vcc based on the voltage of analog voltage signal 70. The quiescent current 45 continuously varies in proportion to the continuously-varying voltage of voltage signal 70. The value of quiescent current 45 is selected so that amplifier 35 will have an optimum current consumption for a selected

linearity over the range of output power levels selected by baseband processor 10 for the RF signal 30 being output by amplifier 35 to antenna 60.

[0033] For example, in one implementation, as the input power of the RF signal 30 provided by preamplifier 25 to amplifier 35 increases (decreases) due to an increase (decrease) in the voltage of the analog voltage signal 50 provided to preamplifier 25 by baseband processor 10, the voltage of voltage signal 70 output by power detector 65 increases (decreases) because the power of the RF signal 30 output by preamplifier 25 and then amplifier 35 was increased (decreased). Based on the increased (decreased) voltage of voltage signal 70, bias circuit 40 proportionally increases (decreases) the quiescent current 45 provided to amplifier 35 from the fixed-level DC voltage source Vcc, thereby obtaining the optimum current consumption at the desired linearity (e.g., Adjacent Channel Power Ratio (ACPR) of –48 dBc or better) for the output power level of amplifier 35 selected by baseband processor 10. The quiescent current 45 sets the linearity. Increasing the quiescent current 45 provides more linearity, and vice versa.

[0034] Bias circuit 40 may be temperature compensated so that the value of quiescent current 45 will not appreciably vary with temperature.

[0035] Amplifier 35 may include only one amplifier stage, or two or more amplifier stages. In the case of a multi-stage amplifier, a single bias circuit 40 can control the quiescent current 45 to one or more of the stages of amplifier 35. Alternatively, a separate bias circuit 40 can be provided for each of the amplifier stages.

[0036] Fig. 2 is a block diagram of an embodiment of automatic-bias amplifier circuit 5 of Fig. 1. In this example, amplifier 35 includes a plurality of amplifier stages, i.e., a first amplifier stage 125 and a second amplifier stage 130, on signal path 21 between input 35a and output 35b of amplifier 35.

[0037] Referring to Fig. 2, amplifier 35 of Fig. 2 includes an input matching network 124 that receives RF signal 30 from preamplifier 25 via input 35a of amplifier 35. Input matching network 124 provides for proper matching of impedances between preamplifier 25 and first amplifier stage 125. First amplifier stage 125 includes an input 125a and an

output 125b. An interstage matching network 127 is on signal path 21 between the output 125b of first amplifier stage 125 and an input 130a of second amplifier stage 130, and provides for impedance matching between the first and second amplifier stages 125, 130. An output 130b of second amplifier stage 130 is provided to output 35b of amplifier 35 through an output impendence matching network 132. Output matching network 132 provides for matching of impedances between second amplifier stage 130 and the antenna 60 (Fig. 1) that is coupled to output 35b of amplifier 35. Input matching network 124, interstage matching network 127, and output matching network 132 may include inductors, capacitors, resistors, and/or other components common to impedance matching networks.

[0038] In Fig. 2, power detector 65 is coupled to signal path 21 at output 35b of amplifier 35. Power detector 65 detects the power of RF signal 30 at the point of coupling to signal path 21, and generates the analog voltage signal 70. Analog voltage signal 70 is reflective of the power of RF signal 30 at the point of sampling. Power detector 65 may detect the power of RF signal 30 by measuring the RF voltage or the RF current.

[0039] Power detector 65 outputs analog voltage signal 70 to downstream elements of feedback loop 37, which in Fig. 2 include an optional voltage divider circuit 105, an optional linearizer circuit 120, and a bias circuit 40 that is coupled to one or more bias inputs of amplifier 35. Other embodiments may include more or fewer circuit elements within feedback loop 37.

[0040] Voltage divider 105 includes resistors 110 and 115. An input of resistor 110 is coupled to output 65b of power detector 65, and receives analog voltage signal 70. The output of resistor 110 is provided to node 117. Resistor 115 is coupled between node 117 and ground 116.

[0041] Voltage divider 105 divides the voltage of voltage signal 70 to a level suitable for use downstream. This has the effect of controlling the amount of quiescent current 45 drawn by amplifier 35, because the amount of quiescent current 45 varies proportionally with the voltage of analog voltage signal 70. Accordingly, the user of automatic-bias

amplifier circuit 5, e.g., a cellular phone manufacturer, can tailor the current consumption and linearity of amplifier 35 by adjusting the resistance values of voltage divider 105.

[0042] In an alternative embodiment, voltage divider 105 may omitted. If necessary, the voltage division function may be incorporated in bias circuit 40.

[0043] In a further alternative embodiment, voltage divider 105 may be replaced by another circuit that shifts the voltage of voltage signal 70, either increasing or decreasing the voltage. For instance, an amplifier circuit could be used to increase the voltage of voltage signal 70, if the particular power detector 65 used did not output voltage signal 70 at a high enough level for downstream use.

[0044] Voltage divider 105 of Fig. 2 is coupled to linearizer circuit 120 of feedback loop 37. Linearizer circuit 120 receives the divided analog voltage signal 70 at its input 120a from node 117 of voltage divider 105. Linearizer circuit 120 is utilized in a case where the particular power detector 65 used (see, e.g., Fig. 4) outputs a non-linear voltage signal 70, as depicted by the graph on the right side of Fig. 2, but the downstream bias circuit 40 (see, e.g., Fig. 6) is linear. Linearizer 120 linearizes analog voltage signal 70, and outputs a linearized analog voltage signal 70 that is approximately linear as a function of power, as depicted by the voltage signal 70 graph on the left side of Fig. 2.

[0045] Linearizer circuit 120 would not be necessary in a case where power detector 65 had a linear output. In other words, a linearizer circuit may or may not be necessary, depending on whether the power detector 65 and bias circuit 40 have matching characteristics.

[0046] The linearizer 120 is coupled to bias circuit 40, and provides the divided, linearized analog voltage signal 70 from its output 120b to bias circuit 40. Bias circuit 40 is coupled to a bias connection point of first amplifier stage 125 of amplifier 35. As discussed below, bias circuit 40 uses the linearized analog voltage signal 70 to control an amount of a variable quiescent current 45 that first amplification stage 125 of amplifier 35 draws from a fixed-level DC voltage source Vcc, thereby optimizing the current

consumption of amplifier 35 for a selected linearity given the output power level previously selected by baseband processor 10 for the RF signal 30 output by amplifier 35.

[0047] In Figure 2, most of automatic-bias amplifier circuit 5, including all parts of amplifier 35, bias circuit 40, power detector 65, and optional linearizer 120, are formed together on a single integrated circuit 135. However, voltage divider 105 of feedback loop 37 is external to the single integrated circuit 135. Such a configuration allows the user, such as a cellular phone manufacturer, to customize the voltage level of analog voltage signal 70, and hence the ultimate value of quiescent current 45, as mentioned above, by adjusting the resistance values or configuration of voltage divider 105. Preamplifier 25 may also be formed on the single integrated circuit 135.

[0048] In an alternative embodiment, all parts of automatic-bias amplifier circuit 5, including amplifier 35, bias circuit 40, power detector 65, linearizer 120, and voltage divider 105, are formed together on a single integrated circuit 135. Preamplifier 25 may also be formed on the single integrated circuit 135.

[0049] Integrated circuit 135 may be formed using silicon, silicon germanium, gallium arsenide, or other conventional process technologies.

[0050] Numerous configurations are possible for power detector 65 of Figs. 1 and 2. In Figure 3, a block diagram of a conventional Schottky diode power detector 200 is depicted as an example of power detector 65 of Figs. 1 and 2. An input 202 of power detector 200 is coupled to signal path 21 at the output 35b of amplifier 35 (Figs. 1, 2), and inputs a sample of RF signal 30. A capacitor 204 is coupled to input 202, and provides for AC coupling. An output of capacitor 204 is provided to diode 206 via node 216. Diode 206 provides half-wave rectification. Between node 216 and ground 211 is a temperature compensation circuit 212 and a diode 214. Temperature compensation circuit 212 provides additional or reduced bias to the input signal in order to compensate for temperature. The output of diode 206 is coupled to a non-inverting input 208a of an operational amplifier 208. Bias circuit 218 also may be coupled to the non-inverting input 208a of operational amplifier 208. The inverting input 208b of operational amplifier 208 is coupled to its output 208c. Hence, operational amplifier 208 is in a

follower configuration. The output 208c of operational amplifier 208 passes analog voltage signal 70 to output 210 of power detector 200.

[0051] An aspect of this exemplary embodiment of power detector 65 is that power detector 65 does not feed the modulation of RF signal 30 into the feedback loop 37, because the power detector 65 has a low frequency response, and thus only weakly tracks the signal envelope. This low frequency response may be achieved through filtering within operational amplifier 208.

[0052] The place where power detector 65 is coupled to signal path 21 of Figs. 1 and 2 may vary. For instance, power detector 65 may be coupled for sampling RF signal 30 at an interior node of amplifier 35 on signal path 21, rather than being coupled to signal path 21 at the output 35b of amplifier 35. By interior node, we mean a node on the signal path 21 that is between, but exclusive of, the input 35a and the output 35b of the multi-stage amplifier 35. For instance, with respect to Fig. 2, power detector 65 may sample at interior nodes such as output 125b of first amplifier stage 125, input 130a of second amplifier stage 130, or output 130b of second amplifier stage 130 prior to output matching network 132, or within interstage matching network 127 or output matching network 132. As an example, Fig. 2 shows an alternative coupling of power detector 65 to signal path 21 at an interior node within interstage matching network 126 of amplifier 35 via line 66.

[0053] Coupling power detector 65 to an interior node of a multi-stage amplifier 35, e.g., within interstage matching network 127, may provide a more accurate determination of the power of the amplified RF signal 30 output by multi-stage amplifier 35. Specifically, impedance changes at the output 35b of amplifier 35 due to changes in the load impedance, e.g., when the antenna 60 (Fig. 1) is brought into contact with an object, may have a lesser effect on power detector 65 when power detector 65 is coupled to such an interior node. In selecting an interior node at which to sample, one may wish to select a node where there is a large voltage variation with power, but that is relatively insensitive to mismatch.

[0054] Of course, sampling RF signal 30 upstream of the output 35b of amplifier 35, e.g., at an interior node of amplifier 35, or even at input 35a, requires that some accounting be made for amplifier characteristics downstream of the point of sampling, such as in the system calibration, or using stored values in memory, software, and/or firmware.

[0055] In an alternative embodiment, power detector 65 is coupled for sampling at a plurality points on signal path 21 of Figs. 1 and 2. For instance, power detector 65 may be coupled for sampling at output 35b and one or more interior nodes of amplifier 35. Alternatively, power detector 65 may be coupled for sampling at a plurality of interior nodes within amplifier 35, and not at output 35b. Alternatively, power detector 65 may be coupled to input 35a of amplifier 35 and to either an interior node within amplifier 35 or to output 35b of amplifier 35. In other words, the plural points on signal path 21 to which the power detector 65 may be coupled for sampling may vary.

[0056] In Figure 4, a multiple node power detector 250 is shown, which may be used in the circuits of Figs. 1 and 2 as power detector 65. For the sake of example, power detector 250 has two sample input lines 251, and thus can sample at RF signal 30 at two nodes on signal path 21 (Figs. 1 and 2), but power detector 250 may be expanded to sample at three or more nodes by increasing the number of sample input lines 251.

[0057] Each of the two sample input lines 251 of power detector 250 includes an input 252 that is coupled for sampling to the signal path 21 (Figs. 1, 2). An input of a capacitor 254 is coupled to input 252, and an output of a capacitor 254 is coupled to an input of a diode 256 through a node 255. Diode 256 provides half-wave rectification. The output of diode 256 is coupled to an input of a summing amplifier 257, as discussed below. Between ground 262 and node 255 is a temperature compensation circuit 264 and a diode 266. Temperature compensation circuit 264 provides additional or reduced bias to the input signal in order to compensate for temperature.

[0058] Summing amplifier 257 is coupled to the output of each of the diodes 256. Summing amplifier 267 includes resistors 258, 260, and 272, and an operational amplifier 270. Resistor 258 is coupled to receive the output of the diode 256 of one of the sample input lines 251 of power detector 250. Resistor 260 is coupled to receive the output of

the diode 256 of the other sample input line 251 of power detector 250. The output of resistors 258, 260 is provided to the inverting input 270b of operational amplifier 270 via node 268. The non-inverting input 270a of operational amplifier 270 is coupled to ground 262. Resistor 272 is coupled between the output 270c of operational amplifier 270 and the inverting input 270b.

[0059] Summing amplifier 257 sums the respective signal outputs of the sample input lines 251 of power detector 250, and outputs a signal (e.g., a DC voltage) that reflects the power of RF signal 30 at the plural nodes being sampled. Sampling a plurality of nodes of amplifier 35, and summing the detected voltages can potentially provide more accurate power detection.

[0060] The ratio of the values of resistors 258 and 260 determines the weight that will be accorded to the outputs of the two sampling input lines 251 of power detector 250. For instance, if the resistances are equal, then equal weight is accorded to the two nodes being sampled by power detector 250. On the other hand, if resistor 260 has a greater resistance than resistor 258, then greater weight would be given to the sample passed through the sample input line 251 that includes resistor 260. Such an unequal weighting may be desirable where one sampling node provides relatively more useful data.

[0061] While a particular summing amplifier 257 is provided in the exemplary circuit of Figure 4, any other known circuits capable of summing the outputs of the plural sample input lines 251 may be used. In addition, instead of using a summing circuit, other circuits may be coupled to the output of the sample input lines 251, to create a different type of voltage signal 70 reflective of the power of RF signal 30. For instance, a differential signal may be produced. That is, in place of summing amplifier 257, a differential amplifier may be used that determines a difference between the signal outputs of the respective sample input lines 251, and outputs a differential signal that reflects the power of the RF signal 30 at the plural nodes being sampled.

[0062] Figure 5 is a schematic diagram of an embodiment of a linearizer circuit 300 that may be used as linearizer 120 of Fig. 1. Linearizer circuit 300 receives the divided analog voltage signal 70 (Figs. 1, 2) at its input 301 from node 117 of voltage divider 105

(Fig. 2), and provides a voltage signal at its output 328 that varies proportionally with analog voltage signal 70 and is approximately linear as a function of the output power of the amplifier. **True?** In this embodiment, linearizer circuit 300 includes a differential amplifier built around NPN transistors 312 and 320.

[0063] In linearizer circuit 300, DC bias is provided to the base of transistor 312 through a NPN transistor 308 and resistor 306. Transistor 308 has its base and collector coupled to DC power supply Vcc through node 310. Accordingly, transistor 308 functions as a diode. Resistor 306 is coupled between the emitter of transistor 308 and the base of transistor 312. The collector of transistor 312 is coupled to power supply Vcc through node 310. Transistor 320 has its base coupled to power supply Vcc through resistor 322, and to ground 324 through resistor 323. The collector of transistor 320 is coupled to output 328, and to power supply Vcc through resistor 318. The emitters of transistors 312 and 320 are coupled to ground 324 through resistors 316 and 321, respectively, and are coupled together through resistor 314.

[0064] In linearizer circuit 300, resistors 316 and 321 define the amount of current that passes through the differential amplifier. In an alternative embodiment, resistors 316 and 321 could be replaced by current sources. Resistor 314 sets the degree of linearity of the differential amplifier. Resistors 322 and 323 set a threshold voltage of the differential amplifier by setting the DC bias at the base of transistor 320.

[0065] In operation, voltage signal 70 passes to the base of transistor 312 via resistor 302 and node 304. The differential amplifier formed by transistors 312 and 320 amplifies a difference between the voltages at the bases of transistors 312 and 320. The DC bias at the base of transistor 320 is fixed, and the voltage at the base of transistor 312 is compared to this voltage. If, for the sake of example, analog voltage signal 70 was zero, all current in the differential amplifier would pass through transistor 320, resulting in a relatively large voltage drop across resistor 318 and a relatively low base level voltage at output 328. As the voltage at the base of transistor 312 passes the voltage at the base of transistor 320 due to the voltage of analog voltage signal 30, the current in the differential amplifier is shifted from transistor 320 to transistor 312. This reduces the current I_1

through resistor 318, and thus increases the voltage of the voltage signal at output 328 beyond the base level mentioned above. As mentioned, the voltage signal at output 328 varies proportionally with the voltage of analog voltage signal 70 and is can be made to be an approximately linear function of the power of RF signal 30 through proper choice of the resistors 314, 316, and 321.

[0066] By adjusting the value of the resistors 314, 316, and 321, the quiescent current 45 (Fig. 6) can be adjusted to match the optimal value as a function of the detected voltage signal 70. If it is necessary that the quiescent current 45 ramp faster with output power, the value of resistor 314 can be reduced, and visa versa. The absolute value of the current I_1, and hence of quiescent current 45, can be adjusted by adjusting the value of resistors 316 and 321. By adjusting the magnitude of current I_1 and the value of resistor 318, the target voltage can be provided via output 328 to the downstream bias circuit of feedback loop 37, as is discussed below.

[0067] Figure 6 is a schematic diagram of an exemplary bias circuit 400, which may be used as bias circuit 40 of Fig. 1. Input 442 of bias circuit 400 is coupled to receive the linearized voltage signal provided at output 328 of linearizer circuit 300 of Fig. 5. Input 442 is coupled to the base of an NPN transistor 446 of bias circuit 400. The collector of NPN transistor 446 is coupled to the fixed-level DC voltage source Vcc. A resistor 450 is coupled between the emitter of transistor 446 and a node 456. Transistor 446 is in an emitter follower configuration. Resistor 454 is coupled between voltage source Vcc and node 456.

[0068] An NPN transistor 460 has its collector and base coupled to node 456 and its emitter coupled to ground 428. A base of an NPN transistor 462 also is coupled to node 456. NPN transistor 462 has its emitter coupled to ground 428, and its collector coupled to the fixed-level DC voltage source Vcc through an inductor 464. The emitters of transistors 460, 462 are coupled to ground 428. NPN transistors 460 and 462 form a current mirror. NPN transistor 462 and inductor 464 are part of amplifier 35 of Figs. 1 and 2, e.g., transistor 462 may be part of first amplifier stage 125 of Fig. 2.

[0069] Thus, bias circuit 400 and amplifier 35 are coupled at node 461 within the current mirror formed by transistor 460 of bias circuit 40 and transistor 462 of amplifier 35. Bias circuit 400 provides a bias input to amplifier 35 at the base of transistor 462. RF signal 30 also is provided to the base of transistor 462 via a coupling capacitor 466 of signal path 21.

[0070] In this exemplary embodiment, transistors 460 and 462 do not have a unity current mirror ratio, but rather have a current mirror ratio set so that much more current passes through transistor 462 than through transistor 460. For instance, transistors 460 and 462 may have a current mirror ratio of between about 1:60 and 1:80. Such a ratio is obtained by varying the size of the emitter junctions of transistors 460 and 462.

[0071] In operation, the bias circuit 400 of Figure 6 receives the linearized analog voltage provided at output 328 of linearizer circuit 300. The resulting voltage at node 442 causes transistor 446 to pass a current from Vcc through resistor 450. The current through resistor 450 continuously varies in proportion to the continuously-varying voltage of voltage signal 70. A fixed-level current also is drawn from voltage source Vcc through resistor 454. The current through resistors 450 and 454 flows through transistor 460 via node 456.

[0072] Hence, the bias circuit 400 generates a current through transistor 460 that has two components: (1) an analog, i.e., continuously-varying, current portion drawn from power supply Vcc through transistor 446 and resistor 450 that varies proportionally with analog voltage signal 70; and (2) a constant current portion drawn from power supply Vcc through resistor 454. In an alternative embodiment, the constant current portion may be omitted by omitting resistor 454.

[0073] As mentioned, transistor 460 forms a current mirror with transistor 462, which is part of amplifier 35 of Figure 1. The current through transistor 460 is mirrored through transistor 462 of amplifier 35. However, because the current mirror ratio of transistors 460 and 462 is about 1:60 to 1:80, transistor 462 draws a much larger quiescent current 45 from the fixed-level DC voltage source Vcc through inductor 464. Quiescent current 45 continuously varies proportionally with the continuously-varying voltage signal 70,

but also includes a fixed component due to the constant-level current drawn through resistor 454. If analog voltage signal 70 was zero, or was below the threshold set by resistors 322 and 323 of linearizer circuit 300 of Fig. 5, then only the constant current drawn through resistor 454 would be mirrored into amplifier 35 as quiescent current 45.

[0074] Accordingly, automatic-bias amplifier circuit 5 of Fig. 1, as exemplified in Figs. 2-6, is self-regulating, in that it automatically regulates in real time the amount of quiescent current 45 drawn from fixed-level supply Vcc by amplifier 35 over the full range of output powers of amplifier 35 specified by baseband processor 10. The magnitude of the quiescent current 45, and hence the linearity of amplifier 35, can be easily adjusted by adjusting the resistances of voltage divider 105, so that a desired balance of linearity and current consumption is obtained. In an embodiment where voltage divider 105 of feedback loop 37 is external to a single integrated circuit that includes all of amplifier 35 and the remainder of feedback loop 37, an adjustment of the magnitude of quiescent current 45 may be accomplished by the user, e.g., a cellular telephone manufacturer, by adjusting the resistance values of voltage divider 105.

[0075] Automatic-bias amplifier circuit 5 of Fig. 1 provides a convenience to users, e.g., cellular telephone manufacturers. Other means of regulating an amplifier in a cellular phone, such as the method described in co-pending application serial number 10/607,959, cited above, use the voltage signal 50 output by baseband processor 10 to optimize the current consumption of the amplifier as a function of output power. In such embodiments, however, a change elsewhere in the system, e.g., such as a substitution of one baseband processor 10 for another or a change within baseband processor 10 could affect voltage signal 50, and thus might require a redesign and/or requalification of the amplifier bias circuit. With the embodiments described above, however, such a change would not require such a redesign or requalification effort, because automatic-bias amplifier circuit 5 self regulates its current consumption as a function of the output power of amplifier 35.

[0076] Figure 7 is a graph of linearity, expressed in terms of ACPR, verses output power for a simulated automatic-bias amplifier circuit at three temperatures: -30 °C, 25 °C, and

85 °C. In this example, the power supply voltage Vcc is 3.4 V. The IS-95 modulation format is used to make the measurements. The design was optimized for CDMA applications. Here, the analog voltage signal was varied as the input power to the amplifier was varied in order to keep the ACPR less than -48 dBc. In this way, no extra quiescent current is used at each output power, and the current consumption is optimized for each output power.

[0077] Figure 8 is a graph of current consumption verses output power for a simulated automatic-bias amplifier circuit at three temperatures: -30 °C, 25 °C, and 85 °C. The analog voltage signal was varied to keep the ACPR less than –48 dBc while minimizing the current consumption. Figure 8 shows that, while output power is increased, current consumption, and therefore power consumption, is increased only minimally through the complete dynamic range. At low power in a standard amplifier with a fixed bias, the current consumption would be much higher with excess linearity. Note that the current has a non-zero floor value, as discussed above, due to a constant-level component.

[0078] . As used herein, the terms "connected," "coupled," or variants thereof, mean any connection or coupling, either direct or indirect, between elements, unless further specified. Further, an element may be "between" two other elements regardless of whether other elements also are between the two elements.

[0079] The detailed description provided above is merely illustrative, and is not intended to be limiting. While the embodiments, applications and features of the present inventions have been depicted and described, there are many more embodiments, applications and features possible without deviating from the spirit of the inventive concepts described and depicted herein.